

High Definition Digital Video Recorder

STK3269

Data Sheets
Version 0.9

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1 Product Overview

STK3269 is a highly integrated digital still camera and digital video recorder controller. STK3269 features high quality image processing and H.264 video compression to deliver excellent quality of still image capture and video recording. Syntek proprietary auto white balance and auto exposure algorithms utilize statistical analysis to deliver precise and pleasing colors.

Integrated microphone amplifier, AGC and audio codec reduce system component count and deliver clear audio recordings at all sound levels.

STK3269 supports major LCD panels via flexible display interface which is also compatible for HDMI transmitter. TV out is available by way of built in TV encoder and DAC.

STK3269 supports most popular non-volatile memory cards with DMA for fast storage. STK3269 supports high speed USB to connect PC. Built in ADC, switch and multiplex circuit make touch panel input possible with minimal system cost.

2 Product Features

H.264 Codec

- Support H.264 baseline profile with maximum 1280x720 image resolution
- Provide bit rate control to improve quality or reduce storage size

JPEG Codec

- Support baseline JPEG with 4:1:1 and 4:2:2 YCrCb sampling in three component images
- Provide loadable quantization table to control picture quality and compression ratio

Image Processing

- Highly pipelined architecture for fast shot to shot performance at high resolutions
- Proprietary color interpolation filter
- Programmable filter to perform brightness/contrast/hue/saturation adjustment and gamma correction
- Advanced edge enhancement and noise removal processing
- Local contrast enhancement
- Skin tone transformation
- Precise digital zooming (12-bit)
- Overlay support (alpha blending, UV keying for special effects)

Sensor Interface

- Support 10MP image sensors at capture mode
- Support 1280x720 image resolution up to 30fps

Seamless interface with most CMOS and CCD image sensor chips
Support of multiple windowed auto focus (AF), auto white balance (AWB) and auto exposure (AE) statistics collection
Lens/sensor optical defect correction
Sensor bad pixel correction

Face Detection

Assist face, facial expression (smile etc.) detection
General object detection is possible with training data change

Graphical Accelerator

Assist image rotation, mirror, and other 2-D logical operations

Audio Processor

Built in headphone amplifier, microphone amplifier and auto gain control (AGC) audio codec
Support MS ADPCM audio compression

8-bit MCU

Turbo8032 compatible micro-controller
Fast fully associative code cache
8KB of zero wait state local SRAM
Integrated with Keil C arithmetic engine for acceleration of 16-bit and 32-bit operations

Memory Control

Support 16-bit width SDRAM, DDR, DDR2 up to 64MB with 4 banks for reduced page break latency

Storage DMA Control

Support Secure Digital (SD and SDIO)
Support Multimedia Memory card (MMC)

USB Interface

Built in USB 2.0 high speed transceiver
Provide 2x bulk IN, 2x bulk OUT, 2x ISO IN, 2x interrupt IN endpoints in addition to 1x default control endpoint

Serial Interface

Support I²C, UART, SPI interfaces

Support SPI flash with DMA

Display Interface

256-color overlay with 4-bit alpha blending
Support major (incl. AU, Topoly) LCD panels with flexible digital interface (8 bit)
Built in TV encoder (NTSC/PAL) and DAC
Support HDMI transmitter interface (8 bit CCIR-656)

General Purpose Interface

General purpose input/output ports for user interface and system control
PWM channels
One pin keypad control (max 16-key)

Miscellaneous Circuit

Automatic TV detection comparator
Battery-low voltage detector
Real Time Clock

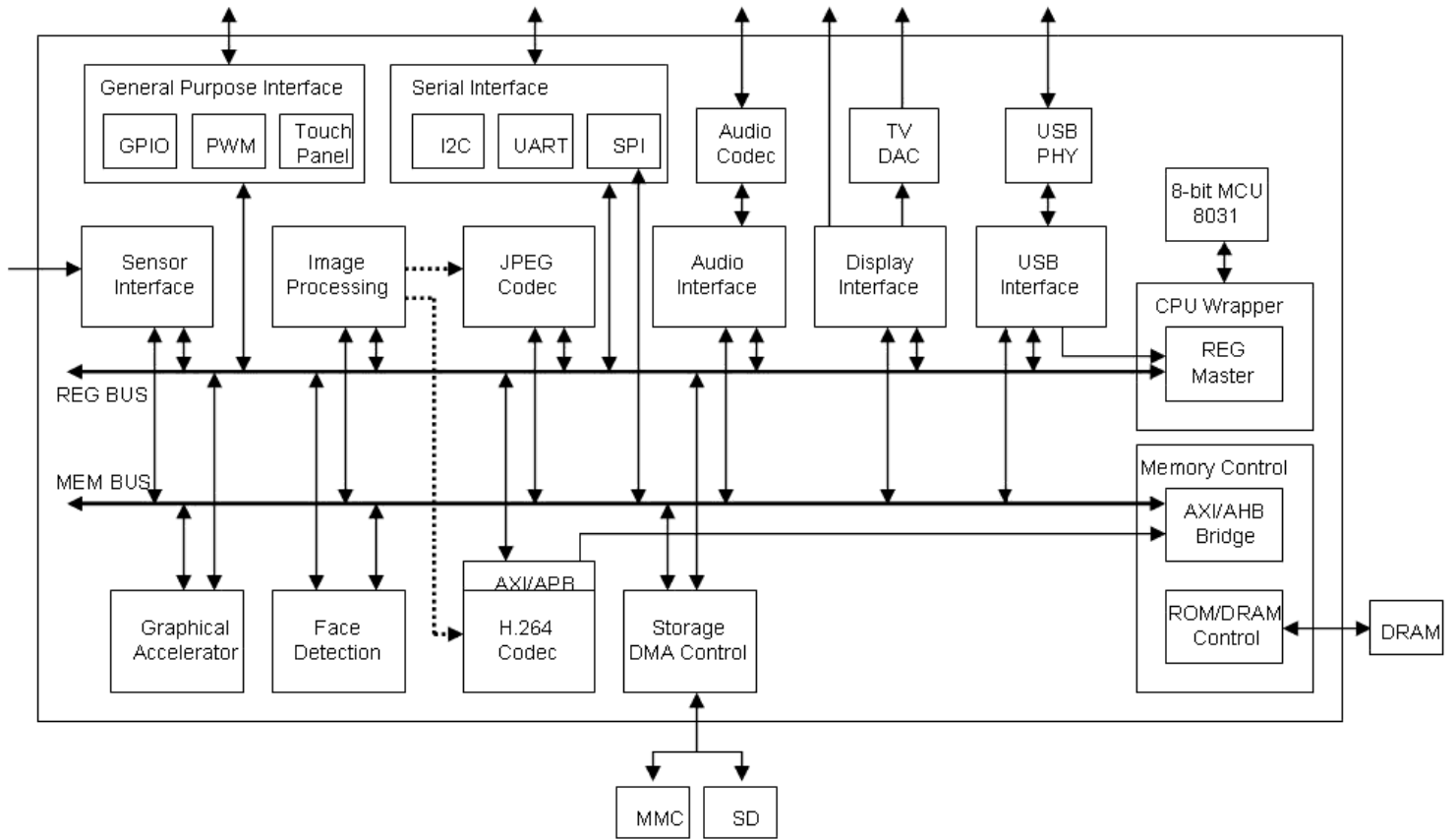
Power management

Dynamic power management by independent module clock frequency setting and gating

Package

168-BGA

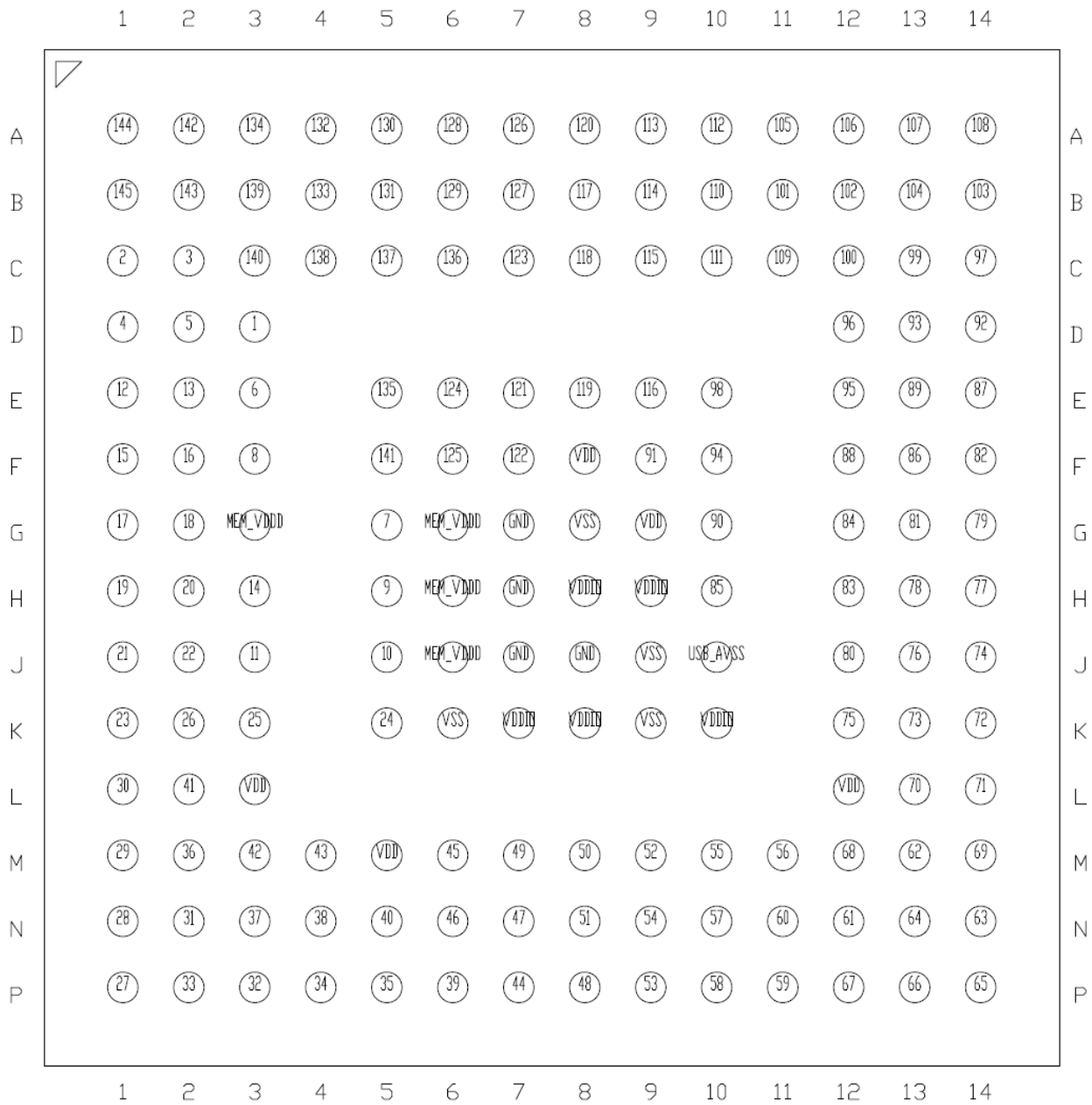
3 Block Diagram



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4 Pin Assignment

TFBGA(HF) 168 (10x10mm)



Pin Description

PIN	NAME	I/O	Attribute	Main Function	Multiplexed Function
A1	MA_2	DO		SDRAM address 2	
A2	MA_0	DO		SDRAM address 0	
A3	MDQS_0	DIO		DDR/DDR2 data strobe 0	
A4	MD_6	DIO		SDRAM data 6	
A5	MD_4	DIO		SDRAM data 4	
A6	MD_2	DIO		SDRAM data 2	
A7	MD_0	DIO		SDRAM data 0	
A8	MSD7	DIO	PU	mass storage data 7	GPIO8[7]
A9	MSD0	DIO	PU	mass storage data 0	GPIO8[0]
A10	SDCMD	DIO	PU	SD card command	GPIO7[7]
A11	SPICS0	DIO	PU	SPI flash chip select 0	GPIO1[0]
A12	SD2D0	DIO	PU	alternate SD card data 0	GPIO1[4]; GPS I-sign in
A13	SD2D1	DIO	PU	alternate SD card data 1	GPIO1[5]; GPS I-mag in
A14	SD2CMD	DIO	PU	alternate SD card command	GPIO14[4]; GPS clock in
B1	MA_3	DO		SDRAM address 3	
B2	MA_1	DO		SDRAM address 1	
B3	MBA_0	DO		SDRAM bank address 0	
B4	MD_7	DIO		SDRAM data 7	
B5	MD_5	DIO		SDRAM data 5	
B6	MD_3	DIO		SDRAM data 3	
B7	MD_1	DIO		SDRAM data 1	
B8	MSD4	DIO	PU	mass storage data 4	GPIO8[4]
B9	MSD1	DIO	PU	mass storage data 1	GPIO8[1]
B10	SDD2	DIO	PU	SD card data 2	GPIO7[5]; UART1 Tx
B11	GPIO0_0	DIO		GPIO0[0]	
B12	GPIO0_1	DIO		GPIO0[1]	
B13	SDCLK	DIO	PU	SD card clock	GPIO7[3]
B14	SDD1	DIO	PU	SD card data 1	GPIO7[2]
C1	MA_4	DO		SDRAM address 4	
C2	MA_5	DO		SDRAM address 5	
C3	MBA_1	DO		SDRAM bank address 1	
C4	MRAS_B	DO		SDRAM row address select	
C5	MCAS_B	DO		SDRAM column address select	
C6	MWE_B	DO		SDRAM write enable	
C7	I2S_SCK	DIO		I ² S bclk	GPIO6[5]
C8	MSD5	DIO	PU	mass storage data 5	GPIO8[5]
C9	MSD2	DIO	PU	mass storage data 2	GPIO8[2]
C10	SDD3	DIO	PU	SD card data 3	GPIO7[6]; UART1 Rx
C11	SDD0	DIO	PU	SD card data 0	GPIO7[4]
C12	GPIO2_3	DIO	PU	GPIO2[3]	I ² C data
C13	GPIO2_2	DIO	PU	GPIO2[2]	I ² C clock
C14	GPIO2_0	DIO		GPIO2[0]	
D1	MA_6	DO		SDRAM address 6	
D2	MA_7	DO		SDRAM address 7	
D3	MVREF	DI		1.25/0.9V reference for DDR/DDR2	
D12	RST_B	DI		system reset	
D13	NANDALE	DIO	PU	NAND flash address latch	GPIO4[3]
D14	NANDCLE	DIO	PU	NAND flash command latch	GPIO4[2]
E1	MCLK	DO		SDRAM clock	
E2	MCLK_B	DO		differential clock for DDR/DDR2 (with MCLK)	
E3	MA_8	DO		SDRAM address 8	

E5	MBE_0	DO		SDRAM byte qualifier 0	
E6	DLL_AVSS	AG		DLL ground	
E7	I2S_SDO	DIO		I ² S dout (playback)	GPIO6[1]
E8	MSD6	DIO	PU	mass storage data 6	GPIO8[6]
E9	MSD3	DIO	PU	mass storage data 3	GPIO8[3]
E10	GPIO2_1	DIO		GPIO2[1]	image sensor clock out
E12	NANDRDY0	DIO	PU	NAND flash ready 0	GPIO4[6]
E13	RTC_AVSS	AG		real time clock ground	
E14	RTC_OSCI	AI		real time clock crystal (oscillator in)	
F1	MSQS_1	DIO		DDR/DDR2 data strobe 1	
F2	MD_8	DIO		SDRAM data 8	
F3	MA_11	DO		SDRAM address 11	
F5	MA_10	DO		SDRAM address 10	
F6	DLL_AVDD	AP		DLL power (1.2V)	
F7	I2S_WS	DIO		I ² S lrck (playback)	GPIO6[4]
F8	VDD	DP		core power (1.2V)	
F9	MSOE	DIO	PU	mass storage output enable	GPIO4[1]
F10	NANDCS0	DIO	PU	NAND flash chip select 0	GPIO4[4]
F12	RTC_OSCO	AO		real time clock crystal (oscillator out)	
F13	RTC_AVDD	AP		real time clock power (1.2V)	
F14	USB_DM	AIO		USB PHY D-	
G1	MD_9	DIO		SDRAM data 9	
G2	MD_10	DIO		SDRAM data 10	
G3	MEM_VDDD	DP		SDRAM power (3.3/2.5/1.8V for SDR/DDR/DDR2)	
G5	MA_9	DO		SDRAM address 9	
G6	MEM_VDDD	DP		SDRAM power (3.3/2.5/1.8V for SDR/DDR/DDR2)	
G7	MEM_VSSD	DG		SDRAM ground	
G8	VSSIO	DG		I/O ground	
G9	VDD	DP		core power (1.2V)	
G10	MSWE	DIO	PU	mass storage write enable	GPIO4[0]
G12	USB_XTALOUT	AO		USB PHY crystal (oscillator out)	
G13	USB_DP	AIO		USB PHY D+	
G14	USB_RES	AO		USB PHY current adjust	resistor to ground
H1	MS_11	DIO		SDRAM data 11	
H2	MD_12	DIO		SDRAM data 12	
H3	MBE_1	DO		SDRAM byte qualifier 1	
H5	MA_12	DO		SDRAM address 12	
H6	MEM_VDDD	DP		SDRAM power (3.3/2.5/1.8V for SDR/DDR/DDR2)	
H7	MEM_VSSD	DG		SDRAM ground	
H8	VDDIO	DP		I/O power (3.3V)	
H9	VDDIO	DP		I/O power (3.3V)	
H10	USB_AVDD12	AP		USB PHY power (1.2V)	
H12	USB_XTALIN	AI		USB PHY crystal (oscillator in)	
H13	CODEC_MICIN	AI		audio codec microphone in	
H14	CODEC_AVDD	AP		audio codec power (3.3V)	
J1	MD_13	DIO		SDRAM data 13	
J2	MD_14	DIO		SDRAM data 14	
J3	MCKE	DO		SDRAM clock enable	
J5	MA_13	DO		SDRAM address 13	
J6	MEM_VDDD	DP		SDRAM power (3.3/2.5/1.8V for SDR/DDR/DDR2)	
J7	MEM_VSSD	DG		SDRAM ground	
J8	MEM_VSSD	DG		SDRAM ground	
J9	VSSIO	DG		I/O ground	

J10	USB_AVSS	AG		USB PHY ground	
J12	USB_AVDD33	AP		USB PHY power (3.3V)	
J13	CODEC_LHPOUT	AO		audio codec left headphone out	
J14	CODEC_VMID	AO		audio codec reference	capacitor to ground
K1	M_15	DIO		SDRAM data 15	
K2	GPIO0_6	DIO		GPIO0[6]	
K3	GPIO0_5	DIO		GPIO0[5]	
K5	GPIO0_4	DIO		GPIO0[4]	
K6	VSSIO	DG		I/O ground	
K7	VDDIO	DP		I/O power (3.3V)	
K8	VDDIO	DP		I/O power (3.3V)	
K9	VSSIO	DG		I/O ground	
K10	VDDIO	DP		I/O power (3.3V)	
K12	CODEC_AVSS	AG		audio codec ground	
K13	TV_VCOMM	AO		TV DAC reference	capacitor to ground
K14	TV_VRSET	AO		TV DAC out current adjust	resistor to ground
L1	SD2D3	DIO	PU	alternate SD card data 3	GPIO1[3]; GPS Q-mag in
L2	CVREF	DIO		image sensor vref in (vsync out)	
L3	VDD	DP		core power (1.2V)	
L12	VDD	DP		core power (1.2V)	
L13	TV_AVDD	AP		TV DAC power (3.3V)	
L14	TV_VOUT	AO		TV DAC out	
M1	SD2D2	DIO	PU	alternate SD card data 2	GPIO1[2]; GPS Q-sign in
M2	CD_5	DIO	PD	image sensor data 5	
M3	CHREF	DIO		image sensor href in (hsync out)	
M4	CCLK	DI		image sensor clock in	
M5	VDD	DP		core power (1.2V)	
M6	LCD_HSYNC	DIO		LCD panel hsync out	GPIO7[1]
M7	LCD_DATA_3	DIO		LCD panel data 3	GPIO5[3]; CCIR656 data 3
M8	LCD_DATA_4	DIO		LCD panel data 4	GPIO5[4]; CCIR656 data 4
M9	LCD_DATA_6	DIO		LCD panel data 6	GPIO5[6]; CCIR656 data 6
M10	GPIO0_3	DIO		GPIO0[3]	
M11	GPIO2_4	DIO		GPIO0[4]	UART0 Rx
M12	TV_AVSS	AG		TV DAC ground	
M13	LCD_DATA_10	DIO	PD	LCD panel data 10	GPIO10[2]; CCIR656 data 10; alternate GPS clock in
M14	BATT_IN	AI		battery low detect in	
N1	GPIO14_5	DIO		GPIO14[5]	
N2	CD_0	DIO	PD	image sensor data 0	GPIO14[0]
N3	CD_6	DIO	PD	image sensor data 6	
N4	CD_7	DIO	PD	image sensor data 7	
N5	CD_9	DIO	PD	image sensor data 9	
N6	LCD_CLK	DIO		LCD panel clock out	GPIO7[0]; CCIR656 clock out; digital MIC clock out
N7	LCD_DATA_EN	DIO		LCD panel data enable out	GPIO5[1]; CCIR656 data 1; digital MIC right channel
N8	LCD_DATA_5	DIO		LCD panel data 5	GPIO5[5]; CCIR656 data 5
N9	GPIO0_2	DIO		GPIO0[2]	
N10	GPIO2_5	DIO		GPIO0[5]	UART0 Tx
N11	LCD_DATA_8	DIO	PD	LCD panel data 8	GPIO10[0]; CCIR656 data 8; alternate GPS I-sign in
N12	LCD_DATA_9	DIO	PD	LCD panel data 9	GPIO10[1]; CCIR656 data 9; alternate GPS I-mag in
N13	LCD_DATA_12	DIO	PD	LCD panel data 12	GPIO10[4]; CCIR656 data 12; alternate GPS Q-mag in
N14	LCD_DATA_11	DIO	PD	LCD panel data 11	GPIO10[3]; CCIR656 data 11; alternate GPS Q-sign in

P1	GPIO0_7	DIO		GPIO0[7]	
P2	CD_2	DIO	PD	image sensor data 2	GPIO14[2]
P3	CD_1	DIO	PD	image sensor data 1	GPIO14[1]
P4	CD_3	DIO	PD	image sensor data 3	GPIO14[3]
P5	CD_4	DIO	PD	image sensor data 4	
P6	CD_8	DIO	PD	image sensor data 8	
P7	LCD_VSYNC	DIO		LCD panel vsync out	GPIO5[0]; CCIR656 data 0; digital MIC left channel
P8	LCD_DATA_2	DIO		LCD panel data 2	GPIO5[2]; CCIR656 data 2
P9	LCD_DATA_7	DIO		LCD panel data 7	GPIO5[7]; CCIR656 data 7
P10	GPIO2_6	DIO		GPIO0[6]	LCD pane data 0; UART2 Rx
P11	GPIO2_7	DIO		GPIO0[7]	LCD panel data 1; UART2 Tx
P12	LCD_DATA_15	DIO	PD	LCD panel data 15	GPIO10[7]; CCIR656 data 15
P13	LCD_DATA_14	DIO	PD	LCD panel data 14	GPIO10[6]; CCIR656 data 14
P14	LCD_DATA_13	DIO	PD	LCD panel data 13	GPIO10[5]; CCIR656 data 13

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Characteristics

Absolute Maximum Rating

RATING	SYMBOL	VALUE	UNIT
DC supply voltage (IO)	V_{dd}	-0.3 to +4.0	V
Voltage, any pin to ground	V	-0.3 to VDD+0.3	V
DC current drain per pin (excluding VDD, VSS)	I	± 10	mA
Operating temperature range	T_A	-40 to +85	$^{\circ}\text{C}$
Storage temperature range	T_{stg}	-65 to +150	$^{\circ}\text{C}$

Electrical Characteristics ($V_{dd} = 3.3\text{v}$, $T_A = -40$ to 85°C)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
DC supply voltage IO (V_{dd} to GND)	V_{dd}	3.00	3.3	3.6	V
DC supply current (@ $V_{dd}=3.3\text{v}$)	I_{dd}		TBD		mA
DC supply voltage core (V_{dd} to GND)	$V_{dd \text{ core}}$	1.19	1.25	1.31	V
DC supply current core (@ $V_{dd \text{ core}}=1.2\text{v}$)	$I_{dd \text{ core}}$		TBD		mA
Suspend mode current (@ $V_{dd}=3.3\text{v}$)	I_{Suspend}		TBD		μA
High level input voltage	V_{IH}	2.0		$V_{dd}+0.3$	V
Low level input voltage	V_{IL}	-0.3		0.8	V
Input current ($V_i=V_{dd} + 0.3\text{v}$ or GND)	I_{IN}	-10	1	10	μA
Input capacitance	C_{IN}			10	PF
3-state output leakage current ($V_o=V_{dd} + 0.3\text{v}$ or GND)	I_{OZ}	-10	1	10	μA
Output capacitance	C_{OUT}			10	PF
High level output voltage (@ $I_{out}=-2\text{mA}$)	V_{OH}	2.4		V_{dd}	V
Low level output voltage (@ $I_{out}=2\text{mA}$)	V_{OL}	0		0.4	V
Crystal frequency (at XIN and XOUT pins)	F_{XLT}	5.88	12	24.012	MHz

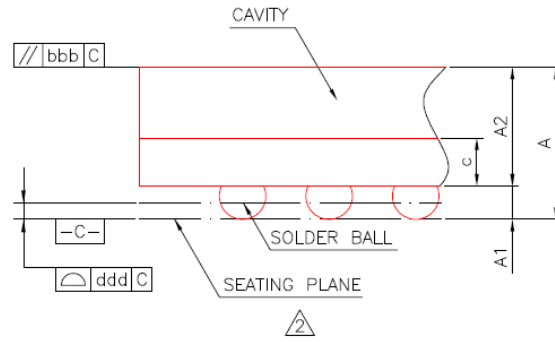
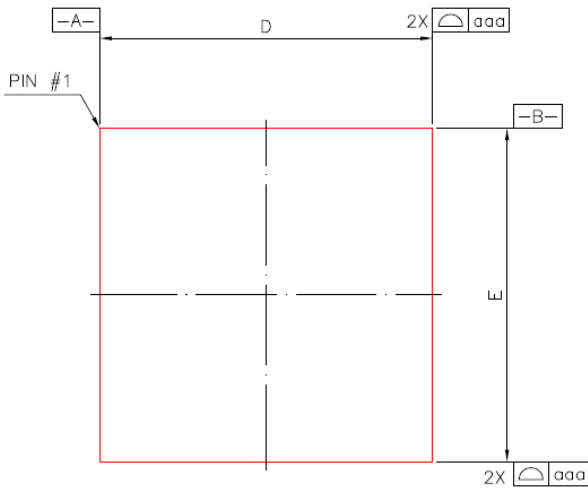
USB VP/VM Pins Electrical Characteristics ($V_{dd} = 3.3\text{v}$, $T_A = -40$ to 85°C)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Differential input sensitivity	V_{DI}	0.2			V
Differential common mode range	V_{CM}	0.8		2.5	V
Output signal crossover voltage	V_{CRS}	1.3		2.0	V
Single ended receiver threshold	V_{SE}	2.0		2.0	V
Static output low (@ $1.5\text{k}\Omega$ pull up to 3.6v)	V_{OL}	0.0		0.3	V

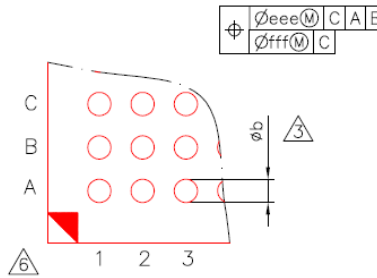
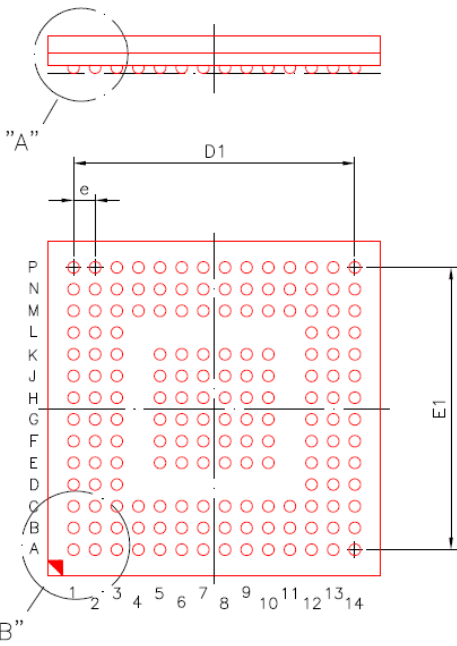
Static output high (@1.5k Ω pull down to GND)	V _{OH}	2.8		3.6	V
Rise time	T _{FR}	4		20	ns
Fall time	T _{FF}	4		20	ns
Output resistance	Z _{DRV}	28		43	Ω
External D+, D- serial resistor	R _S		24		Ω

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5 Package Drawing



DETAIL : "A"



DETAIL : "B"

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	---	8.45	---	---	0.333	---
E1	---	8.45	---	---	0.333	---
e	---	0.65	---	---	0.026	---
b	0.30	0.35	0.40	0.012	0.014	0.016
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.20			0.008		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	14/14			14/14		